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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,944	08/31/2000	Oleg Drapkin	ATI-000152BT	3407

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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,944	DRAPKIN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8,9,12,13,18-20,22,23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9,12,13,18-20,22,23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) *4, 11, 14- 17, 21 and 24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

According to the Election/Amendment filed on 10-07-02, the Applicant elected the species A including claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23, 25, 26 and 27.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18-20, 22, 23 and 25- 27are rejected under 35 U.S.C. 102(b) as being anticipated by Bruccoleri et al. (US Pat. 5,808,488).

Regarding claims 1, 2 and 18, 12 and 22, figure 3 of Bruccoleri shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage (high or low) at input (I+);

introducing a current when (INV2) has high level output with a positive edge of the input signal to charge the parasitic capacitance (Cin) to compensate the current of the input signal charging said parasitic capacitance.

Note that when the input signal voltage is below the threshold voltage of circuit input, the parasitic capacitance (Cin) forming by the gate-source/drain of the transistor(s) of (INV1) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of (INV1) becomes low and the output of (INV2) becomes high thus a current is introduced to the parasitic capacitor (Cin) to compensate for current of the input signal that charge (Cin). The parasitic capacitance (Cin) is across the input and the ground.

Regarding claims 3,19, 13, 23 and 27, figure 3 of Bruccoleri shows a method of reducing distorton of a signal applied to the input of a circuit having a parasitic capacitance wherein, (INV1) detects a direction of change in voltage of the input signal. (INV1) has a high output level and (INV2) has low output level in response to a negative edge input signal. The parasitic

capacitance (Cin) discharges though (INV2) thus, preventing discharging of the parasitic capacitance into the input signal. The parasitic capacitance (Cin) is across the input and the ground.

Regarding claims 5, 6 and 25, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (INV1) for detecting changes of the input voltage; a correction circuit (INV2) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal. Note that when the input signal voltage is below the threshold voltage of circuit input, the parasitic capacitance (Cin) forming between the gate-source/drain of the transistor(s) of (INV1) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, the output voltage of (INV1) becomes low and the output of (INV2) becomes high thus a current is introduced to the parasitic capacitance (Cin) to compensate for current of the input signal that charges (Cin). The parasitic capacitance (Cin) is across the input and the ground. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance.

Regarding claims 8, 9 and 20, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising:

a detection circuit (INV1) for detecting the change of the input signal coupled to the input; and

a correction circuit (INV2) coupled to said detection circuit for compensating for current from the parasitic capacitance (Cin) to be added to the input signal due to a negative edge of the input signal. Note that when a negative edge of the input is detected, the output of the correction circuit (INV2) goes low thus, the current from the parasitic capacitor (Cin) is discharged through (INV2) and the current from the parasitic capacitance is not added to the input signal. It is inherent that the detection circuit (INV1) includes a capacitance directly connecting to one terminal of the parasitic capacitance. The parasitic capacitor (Cin) appears between said input and ground.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2, 5, 6, 12, 18, 22, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Diniz et al. (US Pat. 6,107,868).

Regarding claims 1, 2, 18, 12, 22 and 26, figure 3 of Diniz shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage (high or low) at the input;

introducing a current (64) when a positive edge of the input signal is applied to the gate of (48) to charge the parasitic capacitance not shown and inherently exists between the gate of and the source of (46) to compensate the current of the input signal charging said parasitic capacitance.

Note that when the input signal voltage is below the threshold voltage of transistor (48), the parasitic capacitance forming between the gate-source/drain of the transistor (48) is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (48) is turned on and a current (64) is introduced to the parasitic capacitor to compensate for current of the input signal that charges (Cin). The parasitic capacitance (Cin) is across the input and the ground.

Regarding claims 5, 6 and 25, it is inherent that figure 3 of Diniz shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having

parasitic capacitance, comprising: a detection circuit (48) for detecting changes of the input voltage; a correction circuit (44, 46, 49) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance (not shown, between the gate and the source of transistor 48) due to the positive edge of the input signal. Note that when the input signal voltage is below the threshold voltage of circuit input, the parasitic capacitance forming between the gate-source/drain of the transistor (46) and the parasitic capacitor is charged. When a rising edge of the input signal is detected to be higher than the input threshold, transistor (46) is turned on and current (64) is introduced to the parasitic capacitance to compensate for current of the input signal that charges it. The parasitic capacitance is across the input (gate of 46) and the ground.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 746-5716. The fax phone number for this Group is (703) 308-7722

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
Examiner
12-21-02

TUAN T. LAM
PRIMARY EXAMINER